

## WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit device comprising:  
a first internal circuit including a first MOS transistor operating with  
5 a first voltage higher than a power supply voltage and having a relatively  
thick gate insulation layer;  
a second internal circuit including a second MOS transistor operating  
with a second voltage lower than the first voltage and having a relatively  
thin gate insulation layer; and  
10 restricting means for restricting a voltage transmitted from the first  
internal circuit to the second internal voltage so as to reduce an electric field  
applied to the gate insulation layer of the second MOS transistor.
2. The semiconductor integrated circuit device of claim 1,  
15 wherein the second voltage is one of an external power supply voltage, the  
power supply voltage, a voltage lower than the power supply voltage, and a  
voltage higher than the power supply voltage and lower than the first voltage.
3. The semiconductor integrated circuit device of claim 2,  
20 wherein the restricting means includes a third MOS transistor operating with  
the second voltage and having the relatively thin gate insulation layer.
4. The semiconductor integrated circuit device of claim 3,  
wherein a voltage from the first internal voltage is applied to the second  
25 internal circuit through the third MOS transistor.
5. The semiconductor integrated circuit device of claim 1,

wherein the second MOS transistor is controlled by a row address signal in a semiconductor memory device.

6. The semiconductor integrated circuit device of claim 5,  
5 further comprising an inverter coupled to a connection node of the second and third MOS transistors,

wherein the inverter drives a wordline in the memory device.

7. The semiconductor integrated circuit device of claim 6,  
10 wherein the inverter includes PMOS and NMOS transistors operating with the high voltage and having the relatively thick gate insulation layer.

8. The semiconductor integrated circuit device of claim 1,  
wherein the inverter the restricting means includes a third MOS transistor  
15 operating with the first voltage and having the relatively thick gate insulation layer.

9. The semiconductor integrated circuit device of claim 8,  
wherein the third MOS transistor is controlled by a row address signal in a  
20 semiconductor memory device and the row address signal has the first voltage during the active state.

10. The semiconductor integrated circuit device of claim 9,  
further comprising an inverter coupled to a connection node of the second  
25 and third MOS transistors,

wherein the inverter drives a wordline in the semiconductor memory

device.

11. The semiconductor integrated circuit device of claim 10,  
wherein the inverter includes PMOS and NMOS transistors operating with  
5 the high voltage and having the relatively thick gate insulation layer.

12. A semiconductor integrated circuit device comprising:  
a power terminal receiving a high voltage higher than a power supply  
voltage;

10 a first transistor having a first current electrode coupled to the power  
terminal, a second current electrode coupled to an output terminal, and a  
gate coupled to a first input signal;

a second transistor having a first current electrode coupled to the  
output terminal, a second current electrode, and a gate coupled to a low  
15 voltage lower than the high voltage; and

a third transistor having a first current electrode coupled to the  
second current electrode of the second transistor, a second current electrode  
coupled to a ground voltage, a gate connected to receive a second input  
signal,

20 wherein the first transistor has a relatively thick gate insulation layer,  
and each of the second and third transistors has a relatively thin gate  
insulation layer.

13. The semiconductor integrated circuit device of claim 12,  
25 wherein the low voltage is one of external power supply voltage, the power  
supply voltage, a voltage lower than the power supply voltage, a voltage

higher than the power supply voltage and lower than the high voltage.

14. The semiconductor integrated circuit device of claim 12,  
wherein the first input signal selectively has a high level of the first voltage  
5 and a low level of the ground voltage.

15. The semiconductor integrated circuit device of claim 12,  
wherein the second input signal selectively has a high level of the low  
voltage and a low level of the ground voltage.

10 16. The semiconductor integrated circuit device of claim 12,  
wherein the second input signal includes a row address signal in a  
semiconductor memory device.

15 17. The semiconductor integrated circuit device of claim 16,  
further comprising an inverter coupled to a connection node of the second  
and third transistors,  
wherein the inverter drives a wordline of the semiconductor memory  
device.

20 18. The semiconductor integrated circuit device of claim 17,  
wherein the inverter includes PMOS and NMOS transistors operating with  
the high voltage and each having the relatively thick gate insulation layer.

25 19. The semiconductor integrated circuit device of claim 12,  
further comprising a fourth transistor coupled between the third transistor

and the ground voltage,

wherein the fourth transistor has the relatively thin gate insulation layer.

20. The semiconductor integrated circuit device of claim 19, wherein the fourth transistor is controlled by a block selecting signal in a semiconductor memory device.

21. A semiconductor integrated circuit device comprising:  
a power terminal receiving a high voltage higher than a power supply voltage;

a first MOS transistor having a relatively thick gate insulation layer, the first MOS transistor being coupled between the power terminal and a first internal node;

a second MOS transistor having the relatively thick gate insulation layer, the second MOS transistor being coupled between the power terminal and a second internal node,

wherein the first MOS transistor is controlled by a voltage of the second internal node, and the second MOS transistor is controlled by a voltage of the first internal node;

third and fourth MOS transistors each having a relatively thin gate insulation layer, the third MOS transistor being coupled between the first internal node and a third internal node and the fourth MOS transistor being coupled between the second internal node and a fourth internal node; and

fifth and sixth MOS transistors each having the relatively thin gate insulation layer, the fifth MOS transistor being coupled between the third

internal node and a ground voltage and the sixth MOS transistor being coupled between the fourth internal node and the ground voltage,

wherein gates of the third and fourth MOS transistors are coupled to a low voltage lower than the high voltage; and

5 wherein the fifth MOS transistor is controlled by a first input signal, and the sixth MOS transistor is controlled by an inverted version of the first input signal.

22. The semiconductor integrated circuit device of claim 21,  
10 wherein the first input signal and its inverted version selectively have a high level of the low voltage and a low level of the ground voltage, respectively.

23. The semiconductor integrated circuit device of claim 22,  
wherein the low voltage is one of an external power supply voltage, the  
15 power supply voltage, a voltage lower than the power supply voltage, and a voltage higher than the power supply voltage and lower than the high voltage.

24. The semiconductor integrated circuit device of claim 22,  
wherein the first input signal includes a row address signal and a block  
20 selecting signal in a semiconductor memory device.

25. The semiconductor integrated circuit device of claim 24,  
wherein the first internal node is coupled to a row decoder and driver block of the semiconductor memory device, and the row decoder and driver block selectively drives wordlines of the semiconductor memory device in  
25 response to row address signals.

26. The semiconductor integrated circuit device of claim 24,  
wherein the row decoder and driver block includes row decoder and driver  
circuits each corresponding to wordlines,

wherein each of the row decoder and driver circuits includes:

5 a seventh MOS transistor having a source coupled to the high voltage,  
a drain coupled to a fifth internal node, and a gate connected to receive a  
second input signal; and

eighth and ninth MOS transistors serially coupled between the fifth  
internal node and the ground voltage,

10 wherein each of the seventh and eighth MOS transistors has the  
relatively thick gate insulation layer, and the ninth MOS transistor has the  
relatively thin gate insulation layer; and

wherein the eighth MOS transistor is controlled by a voltage of the  
first internal node.

15 27. The semiconductor integrated circuit device of claim 26,  
further comprising an inverter coupled to the fifth internal node,

wherein the inverter drives a wordline of the semiconductor memory  
device.

20 28. The semiconductor integrated circuit device of claim 27,  
wherein the inverter includes PMOS and NMOS transistors operating with  
the high voltage and each having the relatively thick gate insulation layer.